combination of input data rails and time slots;

apparatus for selecting any of the input bit packs from any of the rails in any of the time slots; and

apparatus for conveying said selected bit pack to any output data position within a combination of output data rails and time slots.

5. (Amended) Apparatus for switching data from any of N input positions arranged as T time slots on R rails to any of M output positions arranged as T2 time slots on R2 rails; comprising:

apparatus for receiving input data arranged as bit packs in T time slots on R rails;

apparatus for selecting data from any of the R rails and latching the selected data during a predetermined time slot to thereby select a bit pack of predetermined R and T values; and

apparatus for conveying said selected bit pack to any output position of predetermined R2 and T2 values.

6. (Amended) Apparatus for switching data from any of N input positions arranged as T time slots on R rails to any of M output positions arranged as T2 time slots on R2 rails, comprising:

M selection blocks, each configured to select a bit pack for a different one of the output positions, and each block including:

apparatus for receiving input data arranged as bit packs in T time slots on R rails;

apparatus for selecting data from any of the R rails and latching the selected data during a predetermined time slot to thereby select a bit pack of predetermined R and T values; and

apparatus for conveying said selected bit pack to any output position of predetermined T2 and R2 values.

11. (Amended) Apparatus for switching data from any of N input positions arranged as T time slots on R rails to any of M output positions arranged as T2 time slots on R2 rails, comprising:

R2 selection blocks, each configured to select a bit pack for a different one of the output positions, and each block including:

apparatus for receiving input data arranged as bit packs on N rails;

apparatus for selecting data from any of the N rails; and

apparatus for conveying said selected bit pack to any output position of predetermined T2 and R2 values.

18. (Amended) The method of claim 17 wherein step (a) comprises the further step of:

(d) selecting a bit pack from any of the N rails.

21. (Amended) The method of claim 20 wherein step (a) further comprises the steps of:

(c) receiving input data arranged as bit packs in T time slots on R rails; and

(d) selecting data from any of the R rails and latching the selected data during a predetermined time slot to thereby select a bit pack of predetermined R and T values.

REMARKS

In the Office Action, the Examiner noted that claims 1-22 are pending in the application and that claims 1-22 stand rejected. By this response claims 1, 5, 6, 11, 18, and 21 are amended and claims 2-4, 7-10, 12-17, 19-20, and 22 continue un-amended.

In view of both the amendments presented above and the following discussion, the Applicants submit that none of the claims now pending in the

application is anticipated under the provisions of 35 U.S.C. §102 or obvious under the provisions of 35 U.S.C. §103. Furthermore, the Applicants also submit that these claims now satisfy the requirements of 35 U.S.C. § 112. Thus, the applicants believe that all of the claims are now in allowable form.

Objections

A. Specification

The Examiner has objected to the amendment filed on 29 January 2002 under 35 U.S.C. 132 "because it introduces new matter into the disclosure." The Applicants respectfully disagree.

In the application the Applicants submit that, "Such a configuration employs a selection block 701 for each of the seven hundred and sixty eight locations in the switch core's output bit map." (See Specification, page 12, line 30, page 13 lines 1-2). The Applicants also note that under the MPEP §2163.06 "...information contained in any one of the specification, claims or drawings of the application as filed may be added to any other part of the application without introducing new matter." (emphasis added).

The Applicants submit that FIG. 7 depicts a physical embodiment for bit maps as the amendment to the specification now describes. In FIG 7 an arrow is drawn from the latch 710 of the selection block 701 to a first position in the Output Bit Map 1 706 indicating that a physical embodiment for a bit map may be realized by employing a selection block, 701, as in Fig. 7, for each of the seven hundred and sixty eight output data bits of the illustrative embodiment. Additionally, the legend under the selection block 701 reads "One of 768 blocks" further illustrating the realization of a physical embodiment of a bit map by employing a selection block, 701, as in Fig. 7, for each of the seven hundred and sixty eight bits of the illustrative embodiment.

In view of the above discussion, it is respectfully requested that these objections be withdrawn.

Rejections

A. 35 U.S.C. § 112

The Examiner has rejected claims 1-22 under the provisions of the first paragraph of 35 U.S.C. § 112 as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 1, 5, 6, 11, 16, and 20

Specifically, the Examiner alleges that, "Claims 1, 5, 6, 11, 16, and 20 use the term 'time slot.' The specification fails to define 'time slot' as it relates to the claimed invention." It is respectfully submitted that the Applicants do in fact define the term time slot as it relates to the claimed invention throughout the specification.

The Examiner alleges that, "The significance, and indeed meaning, of 'time slot' is unclear; one may guess that 32 bits arrive in each 'time slot' or that 32 bytes arrive in each 'time slot'."

The Applicants respectfully submit that the significance and meaning of time slot is clearly defined in the specification. The Applicants disclose that, "...a switch may be made physically smaller if bit-packs can be switched sequentially, using time switching." (See Specification, page 9, lines 27-28). The term bit-packs is also defined in the specification as, "All data channels may have data organized as byte-wide data blocks composed of 1 bit, bit-packs, for example. The switch module includes O switch modules 130-138, where O is the number of bit-packs in a data block. For example, O = 8 when data blocks are 1 byte wide and bit-packs are 1 bit wide, O = 4 when data blocks are 1 byte wide and bit-packs are 2 bits wide, and so on." (See Specification, page 6, lines 27-29; page 7 lines 1-2).

Accordingly, it is evident to one skilled in the art from the disclosure, that the time switching of the present invention is performed on the bit-packs of the system

according to the arrangement of the data in the data channels. The number of bits that arrive in each time slot depends on the size of the bit-packs as defined by the system and also on the number of rails in the system. "The storage areas 412-418 are often depicted, and will be hereinafter, as a switch matrix that may correspond to a combination of time slots and physical connection paths referred to as rails." (See Specification, page 10, lines 11-13). The significance and application of the time slots are further defined in the specification by, "In the following example it is assumed that all 768 STS-1 signals are synchronized to a single clock in a stage prior to the switch comprising the eight switch module." (See Specification, page 11, lines 3-4) (emphasis added). Accordingly, it is evident to one skilled in the art from the disclosure that a time slot is one cycle, or shift, of the described single clock.

The Examiner further alleges, "Furthermore, the apparatus and its method of use, as described in claims 1, 5, 6, 11, 16, and 20, is sufficiently complex that a reasonable detailed description, including a set of detailed drawings, is necessary to enable one of ordinary skill in the art to make or use the invention as claimed." The Examiner bases his rejection on the following statement: "According to Van Hoogenbemt, the selector circuitry is very complex... ."

The Applicants respectfully suggest that the opinion of the drafter of one patent application granted in Jan. 02, 2001 referring to the hardware in another patent application granted in Jan. 05, 1982 that some element is "complex" should not, as a matter of law, be deemed as an accurate characterization and, more particularly, should not be deemed sufficient to reach the conclusion that the instant patent application is not enabled. The test is not "complex" in the opinion of a patent drafter, but sufficient to enable one skilled in the art in the present time. There is no evidence that a) the drafter was skilled in the art and b) that his characterization is even accurate. The Applicants also respectfully submit that the statement in Van Hoogenbemt was taken out of context and additionally does not apply to the selection means claimed in the present invention. Van Hoogenbemt states, "The selector circuitry described in U.S. Pat. No. 4,309,754 is drawn in

FIG. 1 of the U.S. Patent and consists of a microprocessor, control program, storage means, a direct memory access controller, an interrupt controller, a dual port storage memory means, and some other means. The selector circuitry is hence is very complex in hardware." (See Van Hoogenbemt, column 1, lines 35-40) (emphasis added). Van Hoogenbemt states that the selector circuitry of U.S. Pat. No. 4,309,754 is very complex in hardware. The selector circuitry of U.S. Pat. No. 4,309,754 includes a microprocessor, control program, storage means, a direct memory access controller, an interrupt controller, a dual port storage memory means, and some other means. In contrast, the Applicants selector circuitry only contains illustratively a 32 to one multiplexer, an exclusive or gate, and a latch. Accordingly, Van Hoogenbemt admits that, "... when realizing the selector means only by a bank of identical multiplexers and a control unit, the hardware complexity is reduced significantly." (See Van Hoogenbemt, column 2, lines 11-13). Thus even Van Hoogenbemt suggests that a reduction in components reduces the complexity significantly. Furthermore, U.S. Pat. No. 4,309,754 was granted on January 5, 1982. The Applicants may agree that on or before 1982, selector circuitry with the many components listed in the U.S. Pat. No. 4,309,754 may be "sufficiently complex that a reasonable detailed description, including a set of detailed drawings, is necessary to enable one of ordinary skill in the art to make or use the invention as claimed", but now in the year 2002, selector circuitry as the one of the present invention, is well know to one skilled in the art.

In addition, MPEP §2164.04 states, "the examiner has the initial burden to establish a reasonable basis to question the enablement provided for the claimed invention." MPEP §2164.04 continues by quoting the court in In Re Marzocchi, 439 F.2d 220, 224, 169 USPQ 367, 370 (CCPA 1971) ruling, "it is incumbent upon the Patent Office, whenever a rejection on this basis is made, to explain *why* it doubts the truth or accuracy of any statement in a supporting disclosure and to back up assertions of its own with acceptable evidence or reasoning which is inconsistent with the contested statement." The court goes on to say, "However, specific technical reasons are always required." (emphasis added). The

Applicants respectfully assert that selector circuitry, as the one disclosed in the present invention, is well known to one skilled in the art, and the Examiner has not provided "specific technical reasons" as to why or how the disclosure of the selector circuitry is not enabling.

Claims 7, 8, 12, and 13

The Examiner rejected claims 7, 8, 12, and 13 alleging, "Although the specification states, on page 11, lines 22-27, that input and output data bits can be represented by a matrix referred to as a bit map, as depicted in Fig. 6, the specification nowhere offers a physical embodiment for the bit maps." The Applicants respectfully disagree.

In the application the Applicants submit that, "Such a configuration employs a selection block 701 for each of the seven hundred and sixty eight locations in the switch core's output bit map." (See Specification, page 12, line 30, page 13 lines 1-2). The Applicants also note that under the MPEP §2163.06 "...information contained in any one of the specification, claims or drawings of the application as filed may be added to any other part of the application without introducing new matter." (emphasis added). The Applicants submit that FIG. 7 depicts a physical embodiment for bit maps as the amendment to the specification now describes. In FIG 7 an arrow is drawn from the latch 710 of the selection block 701 to a first position in the Output Bit Map 1 706 indicating that a physical embodiment for a bit map may be realized by employing a selection block, 701, as in Fig. 7, for each of the seven hundred and sixty eight output data bits of the illustrative embodiment. Additionally, the legend under the selection block 701 reads "One of 768 blocks" further illustrating the realization of a physical embodiment of a bit map by employing a selection block, 701, as in Fig. 7, for each of the seven hundred and sixty eight bits of the illustrative embodiment.

Therefore, the Applicants submit that claims 1, 5, 6, 11, 16, and 20 as they now stand, fully satisfy the requirements of 35 U.S.C. § 112 and are patentable thereunder.

Furthermore claims 2-4, 7-10, 12-15, 17-19, 21, and 22 depend, either directly or indirectly from claims 1, 5, 6, 11, 16, and 20 and recite additional features therefor. As such and for the exact same reasons set forth above, the Applicants submit that all these dependent claims also fully satisfy the requirements of 35 U.S.C. § 112 and are patentable thereunder.

In view of the above discussion, the Applicants submit that claims 1-22, as they now stand, do not contain any subject matter not described in the specification and do enable one skilled in the art to which it pertains to make and/or use the invention, and hence fully satisfy the requirements of 35 U.S.C. § 112.

B. 35 U.S.C. § 102

The Examiner rejected claims 1-5 under 35 U.S.C. 102(b) as being anticipated by Tocci, Digital Systems: Principles and Applications, 3rd edition (Prentice Hall, Inc. 1985, Pages 388-394). The rejection is respectfully traversed.

In his Response to Arguments, the Examiner alleges that, "...the demultiplexer in Tocci indeed has several inputs. It has one DATA input and several SELECT inputs (see Fig. 9.28). The demultiplexer switches data from one of the several inputs (i.e., DATA input) to any of a plurality of outputs. Any of the SELECT inputs could clearly be substituted for the DATA input." The Applicants respectfully disagree.

Tocci fails to teach or disclose at least the invention as recited in Applicants' amended claim 1 as follows:

> "Apparatus for switching data from any of a plurality of inputs to any of a plurality of outputs, comprising:
>
> apparatus for receiving a plurality of input bit packs organized in a combination of input data rails and time slots,
>
> apparatus for selecting any of the input bit packs from any of the rails in any of the time slots, and

apparatus for conveying said selected bit packs to any output data position within a combination of output data rails and time slots." (emphasis added)

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim" (Lindemann Maschinenfabrik GmbH v. American Hoist & Derrik Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1983)) (emphasis added).

In contrast to the above quoted claim language, the teaching of Tocci specifically states, "... the demultiplexer takes one input data source and selectively distributes it to 1 of N output channels just like a multiposition switch." (See Tocci, Chap. 9, page 388) (emphasis added). The SELECT inputs cannot be used as data channels and even if attempted, only one of the SELECT inputs could be distributed to "1 of N output channels." There is absolutely no teaching of an apparatus for receiving a plurality of input bit packs organized in a combination of input data rails and time slots, or for an apparatus for selecting any of the input bit packs from any of the rails in any of the time slots, and Tocci is in direct contradiction with an apparatus for conveying any selected bit packs to any output data position within a combination of output data rails and time slots.

Therefore, the Applicants submit that amended claim 1 is not anticipated by the teachings of Tocci and, as such, fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Likewise, independent claim 5 recites similar features as recited in claim 1. As such, the Applicants submit that independent claim 5 is not anticipated by the teachings of Tocci and also fully satisfies the requirements of 35 U.S.C. § 102 and is patentable thereunder.

Furthermore, dependent claims 2-4, depend either directly or indirectly from claim 1 and recite additional features therefor. As such and for the exact same reasons set forth above, the applicants submit that none of these claims is anticipated by the teachings of Tocci. Therefore the Applicants submit that all

these dependent claims also fully satisfy the requirements of 35 U.S.C. § 102 and are patentable thereunder.

C. 35 U.S.C. § 103(a)

The Examiner has rejected claims 6,11, and 16-22 under 35 U.S.C. § 103(a) as being unpatentable over the Van Hoogenbemt patent (United States patent 6,169,736 issued Jan. 2, 2001). The rejection is respectfully traversed.

In his Response to Arguments, the Examiner alleges that, "But the claims in no way suggest that such rearrangement is unnecessary for altering the relative order between input and output. Furthermore, the use of appropriate logic circuits to effect the rearrangement noted by Van Hoogenbemt would have been obvious to one of ordinary skill in the art." The Applicants respectfully disagree.

The Applicants submit that the amended claims do in fact suggest that rearrangement is unnecessary for altering the relative order between input and output. Applicants' amended claim 6 specifically recites:

> "Apparatus for switching data from any of N input positions arranged as T time slots on R rails to any of M output positions arranged as T2 time slots on R2 rails, comprising:
> M selection blocks, each configured to select a bit pack for a different one of the output positions, and each including:
> apparatus for receiving input data arranged as bit packs in T time slots on R rails,
> apparatus for selecting data from <u>any</u> of the R rails and latching the selected data during a predetermined time slot to thereby select a bit pack of predetermined R and T values, and
> apparatus for conveying said selected bit pack to <u>any</u> output position of predetermined T2 and R2 values." (emphasis added).

In contrast to the above quoted claim, Van Hoogenbemt teaches an interfacing device "used to extract M outgoing sets of bits (OS1, OS2, ..., OSM) out of N incoming sets of bits (IS1, IS2, ..., ISN) received on said incoming channel (IC), <u>M being an integer number smaller than N</u>... .) (See Van Hoogenbemt, column 9, lines 48-51) (emphasis added). Van Hoogenbemt

teaches an interfacing device for extracting a portion of an input signal to an output channel in the exact arrangement (or a specific order) as the input signal. There is absolutely no teaching, suggestion, or motiviation in Van Hoogenbemt for "M selection blocks, each configured to select a bit pack for any of the output positions." Furthermore, the assertion that "the use of appropriate logic circuits to effect the rearrangement noted by Van Hoogenbemt would have been obvious to one of ordinary skill in the art" does not teach or suggest the Applicants' invention. The rearrangement suggested in Van Hoogenbemt is directed to a configuration that does not reflect the exact arrangement in the output signal as the input signal, but still maintains a specific and continuously implemented order. There is not motivation for "an apparatus for selecting data from any of the R rails and latching the selected data during a predetermined time slot to thereby select a bit pack of predetermined R and T values, and apparatus for conveying said selected bit pack to any output position of predetermined T2 and R2 values." A suggestion that the invention in Van Hoogenbemt can perform the function of the Applicants' invention actually teaches away from the teachings and suggestion in Van Hoogenbemt. Van Hoogenbemt teaches, "In this way, the sequence of outgoing sets of bits may respect the sequence of incoming sets of bits." (See Van Hoogenbemt, column 2, lines 46-47). Although every bit may not be selected, the selection process must still respect the sequence of incoming sets of bits.

As such, the Applicants respectfully submit that Van Hoogenbemt does not teach or suggests or make obvious Applicants' claim 6. Therefore, the Applicants submit that claim 6 fully satisfies the requirements of 35 U.S.C § 103 and is patentable thereunder.

Likewise, independent claims 11, 16 and 20 recite similar features as recited in claim 6. As such, the Applicants submit that independent claims 11, 16 and 22 are not obvious under the teachings of Van Hoogenbemt and also fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

Furthermore, dependent claims 17-19, and 21-22, depend either directly or indirectly from claims 16, and 20 and recite additional features therefor. As such

and for the exact same reasons set forth above, the applicants submit that none of these claims are obvious under the teachings of Van Hoogenbemt. Therefore the Applicants submit that all these dependent claims also fully satisfy the requirements of 35 U.S.C. § 103 and are patentable thereunder.

Conclusion

Thus the Applicants' submit that none of the claims, presently in the application, is anticipated under the provisions of 35 U.S.C. § 102 or obvious under the provisions of 35 U.S.C. §103. Furthermore, the Applicants also submit that all of these claims now fully satisfy the requirements of 35 U.S.C. § 112. Consequently, the applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Eamon J. Wall, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

E J Wall

Eamon J. Wall Attorney
Reg. No. 39,414

Dated: 5/21/02

CUSTOMER #26,291
MOSER, PATTERSON & SHERIDAN, LLP
595 Shrewsbury Avenue, Suite 100
Shrewsbury, New Jersey 07702
732-530-9404 - Telephone
732-530-9808 – Facsimile